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IEEE International Symposium on Circuits and Systems (ISCAS), Baltimore, Maryland, May 2017.



Citation Information (BibTex):

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@INPROCEEDINGS{Amer:2017,
  author="Sherif Amer and Sagarvarma Sayyaparaju and
      Garrett S. Rose and Karsten Beckmann and Nathaniel
      C. Cady",
  title="A Practical Hafnium-Oxide Memristor Model Suitable
      for Circuit Design and Simulation",
  booktitle="Proceedings of {IEEE} International Symposium on
      Circuits and Systems {(ISCAS)}"
  month="May",
  year="2017",
  address="Baltimore, MD, USA"
}
```

# A Practical Hafnium-Oxide Memristor Model Suitable for Circuit Design and Simulation

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***Abstract*—This paper proposes a practical polynomial model for $HfO_2$ memristor fabricated in-house at SUNY Polytechnic Institute. Although there is no shortage of memristor models in the literature, most models are not general and assume specific switching and conduction mechanisms. This is often deemed impractical for circuit designers who wish to develop a model for a specific technology of interest. Thus, circuit designers have sought empirical models that are easily fit to their specific device. The model should be simple, intuitive, and most importantly, fast to converge. The proposed model is based on measurable parameters and matches the experimental data well. The convergence of our model is tested against other models in the literature and shows comparable results. It is also shown that the smoothness of the model around the memristor threshold is critical for fast convergence time.**

## I. Introduction

The memristor concept has emerged as a strong candidate in future computing paradigms. Owing to the peculiar characteristics they exhibit, mainly incremental resistance switching, they have been used in circuit designs such as neuromorphic and security circuits. The search for a physical implementation led to the development of ReRAMs in which those characteristics are leveraged. This surge of memristor-based hardware and applications has instigated the development of several SPICE compatible compact models to be used by circuit designers in their respective applications. Despite the wide variety of existing memristor models that range from simple behavioral models [1], [2] to complex physics-inspired phenomenological models [3], [4], the overwhelming majority of such models have assumed specific switching and conduction mechanisms such as electron tunneling barrier in [3] and exponential ionic drift in [4] which does not render accurate results because the switching mechanisms are likely to be constrained by parasitic effects within the device itself. Also, multiple switching mechanisms can be present in the same device. For example, the model in [3] failed to accurately capture the Set transition operation. Other efforts have been undertaken to develop a general memristor physical model such as in [5], [6]. Yet, the maturity of such models is still questionable and they still contain significant empirical content.

While it is imperative to develop a general physics-based compact memristor model that can model any generic memristive device based on its material properties and geometry, the lack of such a model has encouraged circuit designers to seek empirical models that are easily fitted to measurable parameters extracted from a specific device technology. In [7], Pino $et\ al.$ developed an empirical model for a chalcogenide based memristor. The model is a piecewise model which divides the switching operation into two operation regions: a subthreshold region where the resistance is not allowed to change and an above threshold region where the resistance exhibits an exponential change with the applied voltage. Bayat $et\ al.$ developed a model for $TiO_2$ memristor and proposed a characterization methodology for manufactured devices based on measurable parameters [8]. Their model is entirely based on ad hoc functions inspired by the observed experimental data. In these empirical models, unlike most other models that represent the state variable as the length of the dopant filament, the state variable is the resistance of the device measured at non-disturbing bias conditions (i.e. applying electric stress and measuring the resistance without disturbing the state/resistance of the device). Such a modeling paradigm enables an easier fit to physical data via techniques such as the one in [8].

In this work, an empirical compact model for a $HfO_2$ based memristor designed and manufactured in-house at SUNY Polytechnic Institute in [9] is proposed. The proposed model is an improved version of a simple piecewise linear (PWL) model used to model the same device in [10]. The rest of the paper is organized as follows: section II provides background about memristor modeling and the PWL model previously used for such devices. Section III describes our improved model and compares it to experimental results. Section IV studies the convergence of our improved model and compares it to other models in the literature. Concluding results and future prospects are presented in Section V.

## II. Background

### A. Memristor Modeling

Memristors are recently characterized devices. Their existence was theoretically predicted in 1971 by Leon Chua [11]. Yet, they weren't physically realized until 2008 when HP announced the development of the first physically realizable memristor based on a $TiO_2$ process. In general, memristors are modeled via a system of two coupled equations as theorized by Chua and shown in (1) and (2):

$$I = G(w, V)V, \tag{1}$$

$$\frac{dw}{dt} = f(w, V), \tag{2}$$

where (1) is the port equation that describes the I-V relation of the memristor element and (2) is the state equation that describes the state evolution of the resistance as a function of voltage and the current state of the device. The first memristor model was proposed by HP. It is based on linear ion drift as shown in (3) and (4):

$$V = (R_{on}\frac{w(t)}{D} + R_{off}(1 - \frac{w(t)}{D}))I, \tag{3}$$

$$\frac{dw}{dt} = \mu_v \frac{R_{on}}{D} I, \tag{4}$$

where $w$ is the length of the dopant filament, $D$ is the total length of the memristor, $\mu_v$ is the average mobility of the ions and $R_{on}$ is the minimum resistance of the memristor. These equations effectively model the memristor as two series resistors where $R_{on}$ is the resistance of the doped region, $R_{off}$ is the resistance of the undoped region and $w$ is a state variable that modulates the resistance of the device based on the applied electric field across it.

### B. PWL Model for $HfO_2$ Memristors

A PWL model was originally used for the $HfO_2$ devices considered in this work. The fabricated $HfO_2$ devices were implemented on a 300mm wafer platform based upon the IBM 65nm 10LPe process technology. The here proposed model is adapted from another model developed by McDonald $et\ al.$ in [12] which can be described as follows.

$$\frac{dM}{dt} = \begin{cases} -\frac{\Delta r V(t)}{t_{swp} V_{tp}}, & V(t) > V_{tp} \\ \frac{\Delta r V(t)}{t_{swn} V_{tn}}, & V(t) < V_{tn} \\ 0, & \text{otherwise,} \end{cases} \tag{5}$$

where $M_{t+1} = M_t + \frac{dM}{dt}\Delta t$ which represents the state evolution of the resistance. Since most practical applications operate near the memristor threshold, the port equation is considered to follow simple Ohm's law $V = IM$. The Model also sets the resistance to $LRS(HRS)$ if it goes below/above $LRS(HRS)$. Parameters $t_{swp}(t_{swn})$ are the time to effect a resistance change $HRS$ to $LRS(LRS$ to $HRS)$. $\Delta r$ is the difference between $HRS$ and $LRS$. Parameters $V_{tp}(V_{tn})$ are the positive (negative) thresholds. It is to be noted that all the parameters are measurable and extracted from physical data. The measured parameters for the fabricated $HfO_2$ devices are shown in Table I.

TABLE I: $HfO_2$ memristor parameters

| Parameter | Value |
|---|---|
| $LRS$ | $3k\Omega$ |
| $HRS$ | $45k\Omega$ |
| $\Delta r$ | $HRS - LRS$ |
| $V_{tp}$ | $0.75V$ |
| $V_{tn}$ | $-0.5V$ |
| $t_{swp}$ | $10ns$ |
| $t_{swn}$ | $1us$ |

## III. Proposed Memristor Device Model

While the model presented in (5) is simple, intuitive and tied to experimental data, physical measurements deviated notably from the behavior predicted by the model. Specifically, two features are introduced to improve the model, which are :

- Nonlinear dependence of the change in resistance on the applied voltage
- Resistance saturation

The proposed model is as follows:

$$\frac{dM}{dt} = \begin{cases} -C_{LRS}(\frac{V(t)-V_{tp}}{V_{tp}})^{P_{LRS}} f_{LRS}(M(t)), & V(t) > V_{tp} \\ C_{HRS}(\frac{V(t)-V_{tn}}{V_{tn}})^{P_{HRS}} f_{HRS}(M(t)), & V(t) < V_{tn} \\ 0, & \text{otherwise,} \end{cases} \tag{6}$$

where the $\frac{\Delta r}{t_{sw}}$ term is absorbed in the $C$ coefficient. $f_{HRS}$ and $f_{LRS}$ capture the resistance saturation (commonly referred to as window functions). Equation (7) presents the proposed window function that can be easily fitted to measurable parameters.

$$f(M(t)) = \begin{cases} \frac{1}{1+e^{\frac{M(t)-\theta_{HRS}HRS}{\beta_{HRS}\Delta r}}}, V(t) < V_{tn} \\ \frac{1}{1+e^{\frac{\theta_{LRS}LRS-M(t)}{\beta_{LRS}\Delta r}}}, V(t) > V_{tp} \end{cases} \tag{7}$$

In (7), $M(t)$ is still set to either $LRS$ or $HRS$ once the resistance hits either boundary to ensure it does not exceed the measurable range of resistance.

### A. I-V Fit to Experimental Data

Figure 1 depicts the I-V sweeps for both simulation and experimental measurements. It is readily shown that the polynomial model fits the experimental data better than the linear model. Also, The effect of the window function is emphasized at the bottom left corner of the hysteresis loop as the resistance saturates when it approaches the $HRS$.

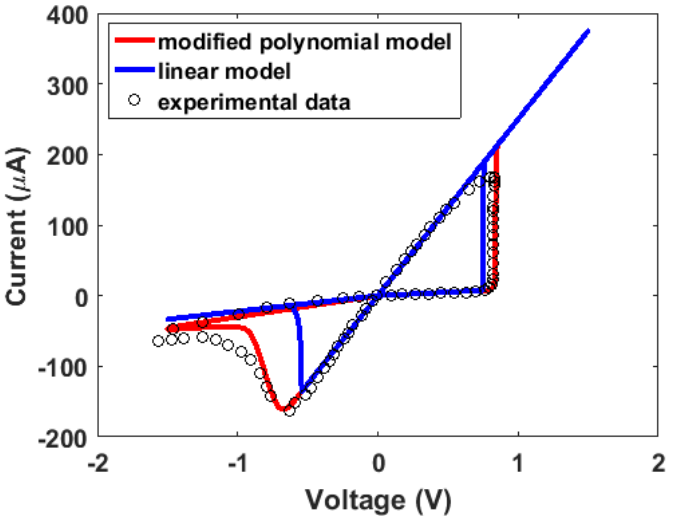


Fig. 1: I-V plots of the linear and polynomial model against experimental data.

### B. Resistance plots against experimental data

An important characteristic of memristors is the resistance saturation near the boundaries (i.e. $HRS$ and $LRS$). Conventionally, resistance saturation has been captured using window functions. In this work, we use our proposed window function with two fitting parameters $\theta$ and $\beta$ as shown in Fig. 2. Fig. 3 depicts the evolution in resistance against time for both models. Starting from LRS of $3k\Omega$, eight consecutive 10ns pulses of equal amplitude were applied yielding an incremental resistance from $LRS$ to $18k\Omega$. As expected, experimental data shows that the pulse response plateaus. The voltage dependent term in both (5) and (6) is a constant in this experiment since the applied pulse amplitude does not change. This emphasizes the effect of resistance saturation which is reasonably captured by the proposed window function in (7). On the other hand, the linear model predicts a constant increase in the resistance.The fitting parameters used are $\theta_{HRS} = 0.4$ and $\beta_{HRS} = 0.05$.

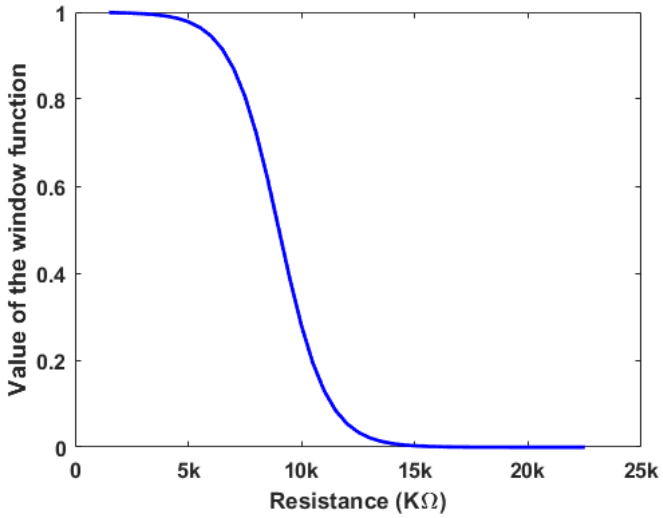


Fig. 2: Proposed window function $f_{HRS}$ with $\theta_{HRS} = 0.4$ and $\beta_{HRS} = 0.05$.

## IV. Model Convergence

An important criterion in circuit simulation is how well the model converges for large networks [13]. Specifically, memristor-based networks such as neuromorphic circuits or ReRAM implementations are typically dense networks. Thus, the convergence of the proposed model is assessed and compared to other relevant models in the literature via a benchmark circuit proposed in [14] in which the authors compare the performance of different models for large memristive systems. The advantage of this circuit is:

- It includes no other elements other than memristors. Thus, the convergence of the simulation is a strong function of the memristor model
- All nodes are updated every simulation cycle and, accordingly, all memristors are updated.

While the circuit might not be typical of a practical application, its structure helps in stressing the model. The circuit has 840

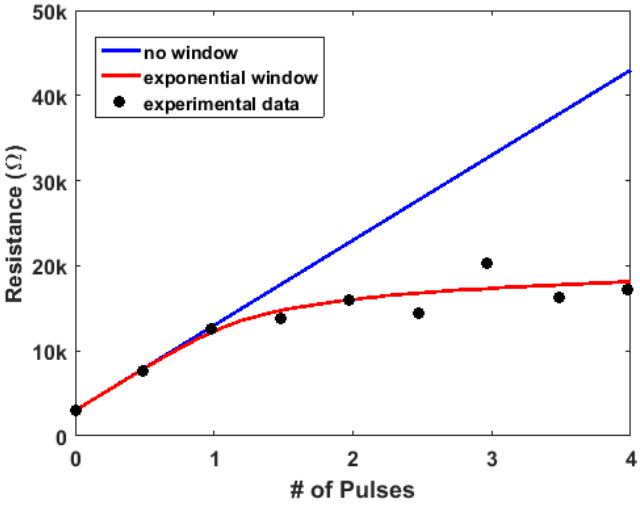


Fig. 3: Resistance vs.time plots of both models against experimental data.

memristors. A sinusoidal signal of $10kHz$ was applied at the input and the simulation was run for different transient times according to the applied test. All models are implemented in Verilog-A and simulations were run on Spectre simulator. The proposed benchmark is depicted in Fig. 4.

The results of the simulations show that there are two main factors that affect the simulation time: (1) the smoothness of the function around the memristor threshold and (2) the non-linearity of the model associated with the complexity of the mathematical function used in the model (i.e. linear, exponential..etc).

In [14], the models under test did not have a threshold. However, the high non-linearity around the threshold of the memristor associated with the switching process is inherently incorporated in the mathematical function. On the other hand, several models in the literature, including the models studied in this paper, explicitly force a threshold via a piecewise implementation of the model. In these models, the resistance of the memristor is not allowed to change at all below the threshold while the model function is applied above the threshold. This might create a discontinuity in the derivatives which prolongs the convergence time. In order to illustrate this point, two comparisons were made. First, the simulation time of the PWL model in (5) is compared against the proposed model in (6). $P_{HRS}$ and $P_{LRS}$ where set equal to 1 to ensure that both models are linear under this test. Second, the model in [7] was modified such that the exponential term $e^x$ was replaced by $e^x - 1$. The results are shown in Table II.

TABLE II: Effect of the model smoothness on the simulation time

| Model | Pino | Modified Pino | PWL | Proposed |
|---|---|---|---|---|
| Simulation time | 4m 24s | 1m 28s | 4m | $<$ 10s |

The significant difference between the models simulation

time is primarily due to the abrupt change at the memristor threshold which is mitigated by subtracting 1 from the exponential term in the Pino model and subtracting $V_t$ in the proposed model (numerator of (6)). This provides smoother transition at the memristor threshold. The apparent difference in simulation time between the modified Pino model and the proposed model is attributed to the non-linearity of the model (Pino model is an exponential model while the proposed model in this test is assumed linear).

To test the effect of the model non-linearity on the simulation time, the proposed model was simulated with different powers as shown in Table III.

TABLE III: Effect of the model non-linearity on the simulation time

| $P_{HRS}/P_{LRS}$ | 1 | 3 | 5 |
|---|---|---|---|
| Simulation time | 50s | 3m 58s | 3m 50s |

It is readily shown that the simulation time increases as the model non-linearity increases. While it was expected that the simulation time for $P_{HRS}/P_{LRS}$ of 5 would be larger than 3 due to the higher non-linearity, it can be seen from (6) that the higher power provides more smoothness at the threshold which accelerates the convergence.

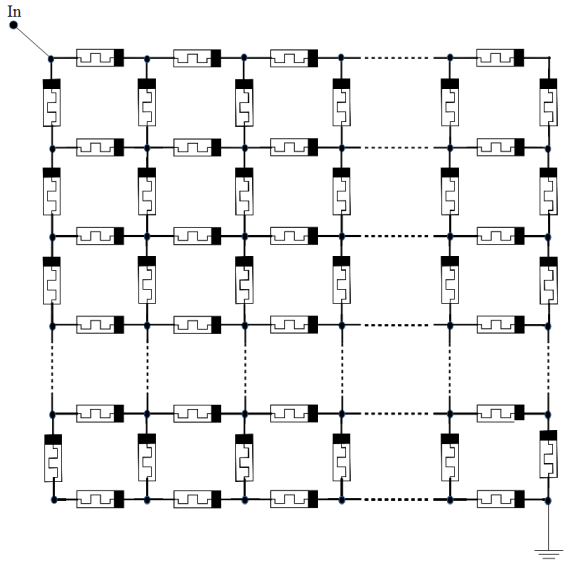


Fig. 4: Benchmark circuit for the convergence test [14].

## V. Conclusion

In this work, a practical memristor model for $HfO_2$ fabricated in-house at SUNY Polytechnic Institute was presented. The model is adapted from an earlier PWL model developed for the same device. The proposed polynomial model captures the inherent non-linearity in the device that the earlier model failed to capture. Our model is simple, intuitive and uses the instantaneous resistance of the device as the state variable which makes it more amenable for fitting against experimental data. Simulation results show a reasonable model convergence compared to other relevant models in the literature. The improvement was achieved primarily due to the smooth transition at the memristor threshold.

## Acknowledgment

The authors would like to thank Dr. Mark Dean, Gangotree Chakma, Mesbah Uddin and Md. Badruddoja Majumder at the University of Tennessee, Knoxville for interesting and useful discussions on this topic.

This work was funded in part by the Air Force Research Laboratory, Information Directorate under award number FA8750-16-1-0065.

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