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A Multi-Driver Write Scheme for Reliable and Energy Efficient 1S1R ReRAM Crossbar Arrays

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Abstract

This work proposes a reliable and an energy efficient Multi-Driver write scheme for 1S1R ReRAM crossbar arrays. The IR drop induced by the line resistance results in a significant degradation of the delivered voltage across the selected cell. This degradation hampers the write window and may cause write disturbance. It also increases the write latency resulting in increased energy consumption of the crossbar array. To this end, the Multi-Driver write scheme, proposed in this work, improves the voltage delivered across the selected cell via reducing the effective line resistance. This enhancement in voltage delivery improves the write margin. In addition, it allows for reducing the write voltage that reduces both write disturbance and energy consumption of the crossbar array. It is shown that for large crossbar arrays, Multi-Driver write scheme outperforms the conventional write approach while its gains are suppressed for small crossbar arrays.

Keywords

Crossbar, Memory, Reliability, Energy, Power, Latency, 1S1R

1. Introduction

Memory systems are indispensable building blocks in modern VLSI systems. With Moore's law plateauing, new novel nanoelectronic structures have been proposed based on emerging devices that are thought to revolutionize memory design. In particular, Crossbar arrays based on resistive switches such as MRAM, PCRAM and RRAM are thought to be ideal for memory arrays due to their nonvolatility, inherent dense structure and, ideally, $4F^2$ footprint. Amongst the three nonvolatile memory devices, RRAM devices (i.e. Transition Metal Oxide resistive switches) have been predominately adopted by the research community owing to their promising characteristics such as CMOS compatibility, low operating voltages and decent state retention [1].

Due to sneak path currents, however, ReRAM arrays require a selector device for every cell to circumvent those unwanted currents [2]. Conventionally, a FET device is integrated with the RRAM device leading to the de-facto ReRAM technology: 1T1R arrays. However, the introduction of the FET device (i.e. 1T) prohibits the $4F^2$ cell footprint and, more importantly, limits the Back-End-Of-Line (BEOL) compatibility which is a major advantage of resistive crossbar arrays [1]. To this end, researchers have started exploring new selector devices that exhibit high ON/OFF ratio to suppress sneak paths but, at the meantime, can be implemented in the BEOL portion of the process flow. Several devices have been proposed each with its merits and demerits. A comprehensive review of such selector devices can be found in [2]. ReRAM arrays based on BEOL compatible selector devices are typically referred to as 1S1R arrays.

Several Read/Write schemes have been proposed in the literature to ensure efficient and reliable operation of 1S1R arrays [3] and [4]. The write operation, in particular, consumes significant energy which impacts the performance of 1S1R arrays. This degradation is primarily due to IR drop across the interconnect which hampers both the write latency and power. In [5], energy models were developed for both V/2 and V/3 bias schemes and a hybrid bias scheme was developed for energy efficient write operation. In [6], cross-layer design techniques were proposed to improve the energy efficiency of 1S1R ReRAMs where both circuit and architectural solutions were proposed.

This work proposes a Multi-Driver write scheme that enhances the delivered voltage across the selected cell via reducing the effective line resistance. It is shown that this improvement in voltage delivery enhances the reliability of the write operation through reducing the disturbance voltage and boosting the write window. In addition, due to the exponential relation between the applied voltage across the 1S1R cell and the device switching, enhancement of the delivered voltage significantly improves the write latency, thus, improving the write energy of the crossbar array.

Section 2 provides background about memory and selector devices as well as crossbar arrays. Section 3 proposes the Multi-Driver write scheme and investigates its impact on both reliability and performance of the crossbar array. Section 4 presents a case study for 512X512 crossbar array and section 5 presents the conclusions.

2. Background

This section reviews the device characteristics of RRAM switches as well as their SPICE modeling. Basics of Crossbar arrays such as read/write schemes and sneak paths are also briefly reviewed.

2.1. RRAM Device Model

Several RRAM device models have been proposed over the past decade that vary from physics-based models to behavioral models. Both approaches often describe the device dynamics in terms of an internal state variable that controls the resistance evolution which may not necessarily reflect measurable parameters. Experimental data, however, often report the instantaneous current as a function of the applied voltage from which the instantaneous resistance can be extracted. The functional relation between the device resistance and the state variable is then left for the modeler to interpret which is, in most cases, challenging!

The compact model used in this work was initially proposed in [7] which uses the instantaneous resistance as the state variable and parametrized in terms of measurable quantities that experimentalists report. The model is based on four measurable parameters, namely: High Resistance State *HRS*, Low Resistance State *LRS*, positive (negative) threshold voltages V_{tp} (V_{tn}) which correspond to the device switching from *HRS* to *LRS* (*LRS* to *HRS*). The analyses presented thereafter are based on these four parameters; please see [7] for more details about the model.

2.2. Selector Device Model

Several works have proposed selector models such as [4]. The model proposed in this work, however, adopts the same structure of the RRAM model such that it reflects actual physical measurable parameters that are readily extracted from V-I sweeps. The proposed selector model is described as follows:

$$\frac{dR}{dt} = \frac{\Delta r}{t_{sw}}\left(e^{\frac{|V(t)|-V_{th}}{V_S}} - e^{\frac{V_{on}-|V(t)|}{V_R}}\right) \quad (1)$$

where $|V(t)|$ is the absolute voltage applied across the selector device, Δr is the difference between *HRS* and *LRS* , V_{th} and V_{on} are the threshold and on voltage, respectively, t_{sw}, V_S and V_R are fitting parameters. The use of the rate of change of the resistance is motivated by the memristive dynamics and the hysteresis exhibited by most selectors reported in the literature. The selector device is normally initialized to *HRS*. As the voltage across the device hits V_{th}, the device switches to *LRS* and remains at *LRS* as long as the voltage across the device exceeds V_{on} while it relaxes back to *HRS* otherwise.

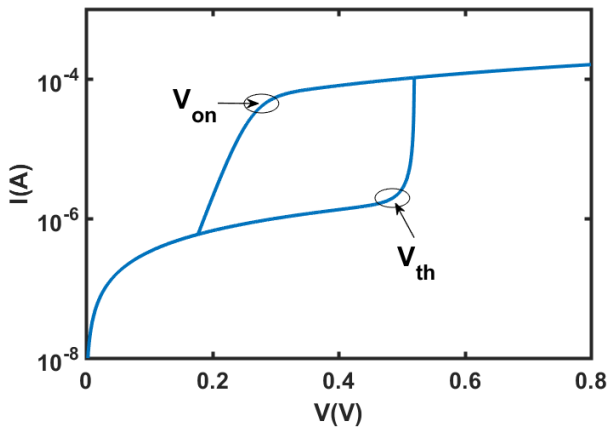

Figure 1: Selector Device V-I characteristics

2.3. 1S1R crossbar arrays

Fig 2 depicts the typical structure of a 1S1R crossbar array. A series combination of the memory element (1R) and the selector element (1S) exists at every intersection point connecting the rows and columns of the crossbar array while an interconnect resistance R_{int} exists between every two adjacent cells. At the periphery, row and column drivers are employed to execute SET and RESET operations. In addition, a sensing circuit consisting of a load resistance and a sense amplifier is used for the read operation.

Several bias schemes have been proposed during the write operation. The traditional approach is to apply write voltage and ground across the row and column of the selected cell while leaving all other rows and columns floating. This approach, despite its simplicity, suffers severe write disturbance of the unselected cells due to sneak path currents deeming this approach unpractical. Two bias schemes are conventionally used commonly referred to as the V/2 and the V/3 bias schemes. In the V/2 write scheme, the unselected rows and columns are biased with half the write voltage while in the V/3 write scheme the rows are biased with two thirds of the write voltage and columns are biased with one third of the write voltage. These techniques eliminate the sneak path problem yet the row and column of the selected cell incur a voltage drop of half and third the write voltage for the V/2 and V/3 bias, respectively. In this work, we adopt the V/2 bias scheme due to its lower power consumption [4]. Fig 3 depicts the crossbar array under the half-bias scheme. The circled cell is the selected cell while the cells enclosed in rectangles are biased with half the write voltage and, therefore, referred to as the half-selected cells. All other unselected cells have no voltage bias across them.

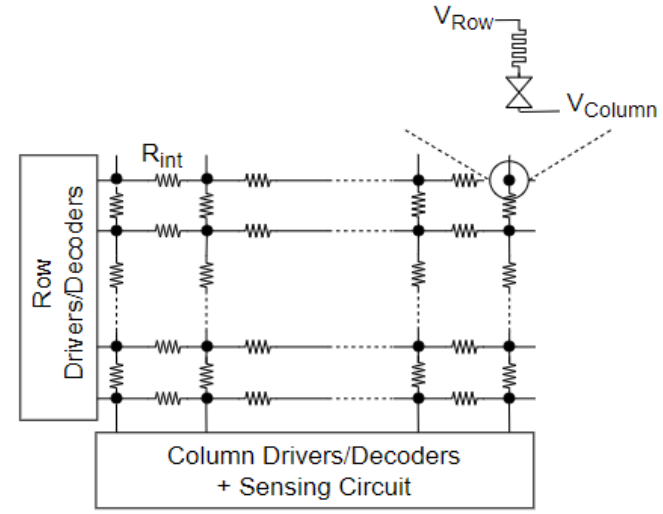

Figure 2: 1S1R crossbar array

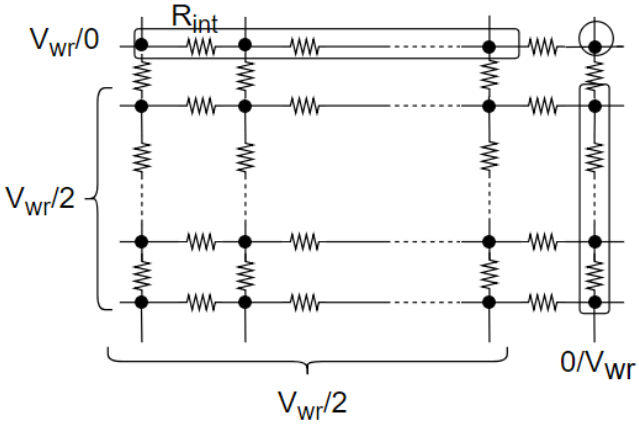

Figure 3: Half-bias scheme of crossbar arrays

3. Multi-Driver write scheme

Resistive Drop across the interconnect (commonly referred to as IR drop) significantly degrades the reliability and performance of the crossbar array which are two major pillars of VLSI systems. In this work, the write window [4] will be used as a figure of merit to evaluate the signal integrity and reliability of the crossbar array during the write operation. On the other hand, the write energy [5] (can be viewed as power-delay product) will be used to assess the performance of the write operation.

In this work, a Multi-Driver write scheme is proposed to improve the reliability and performance of 1S1R ReRAM arrays. Multi-Driver design approach reduces the effective interconnect length during write operation thereby reducing voltage degradation. This reduction enhances both signal integrity and energy consumption. Section 3.1 explains the circuit concept behind the Multi-Driver design while sections 3.2 and 3.3 present simulation results for both figures of merit.

3.1. Circuit concept

Fig 4 depicts the circuit design of the Multi-Driver design scheme. Unlike conventional write scheme where the array is driven from one side only (one for the row and the other for the column), the Multi-Driver scheme drives the array from two sides for the Dual-Driver and from all four sides for the Quad-Driver. In the case of the Dual-Driver approach, the drivers can be either placed on both sides of the rows or the columns.

In this work, we follow the worst-case cell analysis as in previous works where the cell farthest from the row and column drivers suffers the most voltage degradation. For an N X N crossbar array, (here we consider square arrays as in other works), the worst-case cell experiences a line resistance of (N-1) rows and (N-1) columns. An interconnect resistance of 2.5 Ohm [8] is used in this work. While the line resistance can be ignored for small crossbar arrays, its impact becomes pronounced as the array size gets larger. One can readily see that for arrays with hundreds of rows and columns, the line resistance becomes comparable with the LRS value of the memory cell.

In the Multi-Driver scheme, however, the line resistance is reduced to N/2-1 columns and N-1 rows in the Dual-Driver approach while it is further reduced to N/2-1 rows and N/2-1 columns for the Quad-Driver approach, of course at the expense of larger area occupancy. Fig 5 presents the circuit model of the Multi-Driver scheme. First, delta-to-wye conversion is employed to reduce the resistive ladder between the row (column) drivers and the selected cell into a simple T-model consisting of a horizontal resistance R_H and a vertical resistance R_V that together model the impact of the line resistance. Fig 6 shows the impact of the array size on both R_V and R_H.

In the Single-Driver approach (conventional approach), the equivalent circuit of the crossbar array corresponds to the circuit consisting of the series combination of A_{row}, R_{cell} and A_{column}. In the Dual-Driver approach, however, A_{row} is connected in parallel with B while in the Quad-Driver approach, A_{row} and A_{col} are connected in parallel with circuits B and C, respectively. Hence, the equivalent line resistance of the crossbar array decreases as one goes from Single, Dual to Quad drivers. This decrease in the equivalent resistance improves voltage delivery across the worst-case cell.

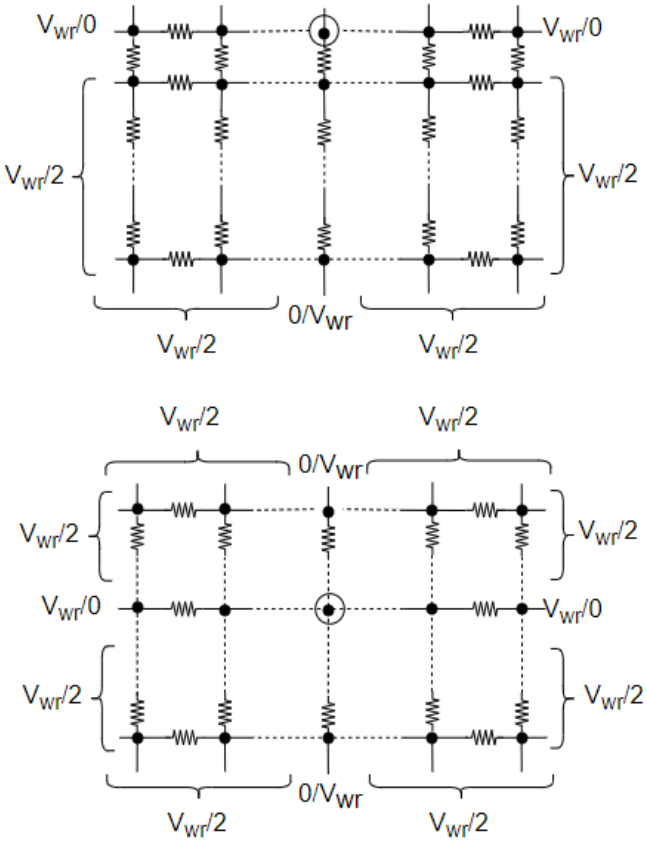

Figure 4: 1S1R equivalent circuit for Dual-Driver (top) and Quad-Driver (bottom).

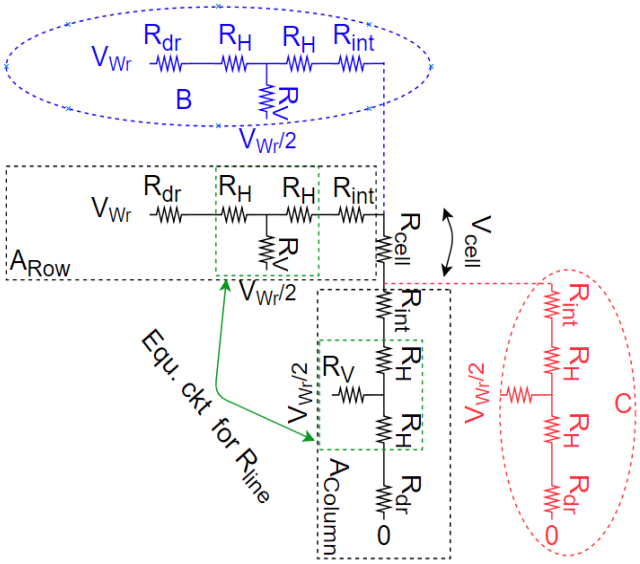

Figure 5: Equivalent circuit of the crossbar array under the Multi-Driver scheme

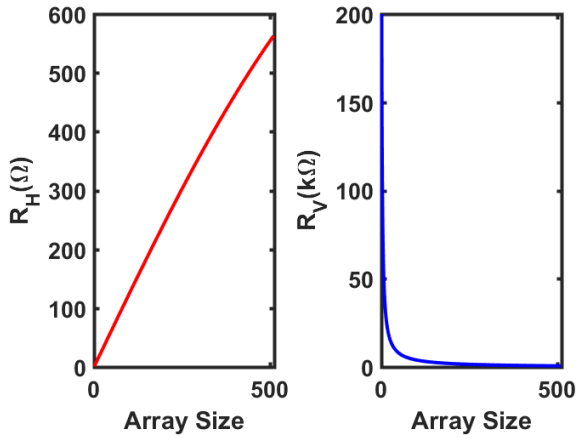

Figure 6: Effective line resistance vs. array size

3.2. Reliability of the Multi-Driver write scheme

To ensure signal integrity during write operation, sufficient voltage should be delivered across the selected cell: higher than the cell threshold voltage. The cell threshold should not be confused with the individual threshold voltage of either the selector or the memory element. To effect a successful write operation, both memory and selector elements need to switch and the minimum voltage required to achieve this condition is referred to, in this work, as the cell threshold. Due to IR drop, however, especially for large arrays, the delivered voltage might drop significantly below the write voltage hampering the write operation reliability.

The write disturbance voltage is defined as the maximum voltage dropped across the unselected cell. In the V/2 biasing scheme, the cell closest to the write driver suffers the maximum disturbance where $\boldsymbol{V_{dis} = V_{wr}/2}$. In reality, the disturbance value is slightly lower than $\boldsymbol{V_{wr}/2}$ due to the drop across the driver resistance but here we take a conservative approach by considering the maximum disturbance. The write window is defined as the difference between the voltage delivered across the selected cell $\boldsymbol{V_{cell}}$ and the maximum disturbance voltage across the unselected cell $\boldsymbol{V_{dis}}$. The Normalized Write Window (NWW) can be expressed as follows:

$$\boldsymbol{NWW = \frac{V_{cell} - V_{dis}}{V_{dis}}} \quad (2)$$

Fig 7 depicts the Normalized Write Window for different array sizes. For small array sizes, the NWW is almost unity (maximum NWW) for all three schemes since IR drop is minimal. As the arrays size grows, however, the difference amongst the different write schemes becomes apparent. Due to lower effective line resistance, the voltage delivered to the selected cell is higher when more write drivers are employed thereby boosting the NWW.

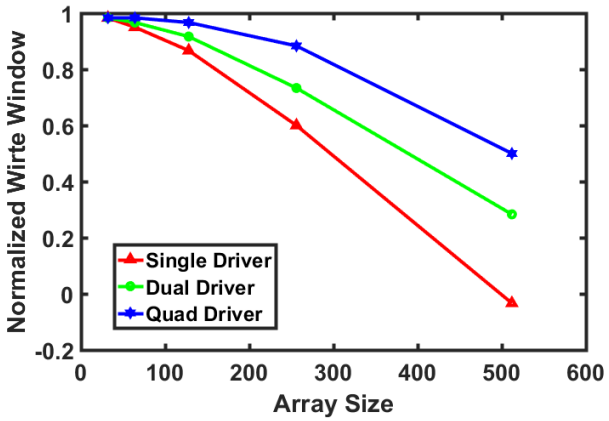

Figure 7: Write window vs. array size

3.3. Energy efficiency of the Multi-Driver write scheme

Another advantage of the Multi-Driver write scheme is manifested in improving the energy efficiency of the crossbar array. The main idea rests in the exponential relationship between the switching time and the applied voltage across the 1S1R cell. Both selector and memory elements exhibit an exponential relation with the applied voltage across them. Hence, employing a Multi-Driver scheme enhances the voltage delivered across the selected cell via reducing the effective line resistance which ultimately reduces the write latency of the 1S1R cell. Although, the write power increases as more drivers are employed, it does not increase as aggressively as the latency decreases. Hence, the write energy is reduced. Fig 8, 9 and 10 depict the write power, write latency and write energy, respectively, for different array sizes. As the array size increases, the difference amongst the three write schemes become more pronounced. For small sizes, however, the driver resistance of the peripheral circuitry dominates the line resistance and, hence, no significant difference is observed. It is readily shown that the write latency scales more aggressively as more drivers are employed than the write power which, subsequently, results in a significant improvement in the write energy.

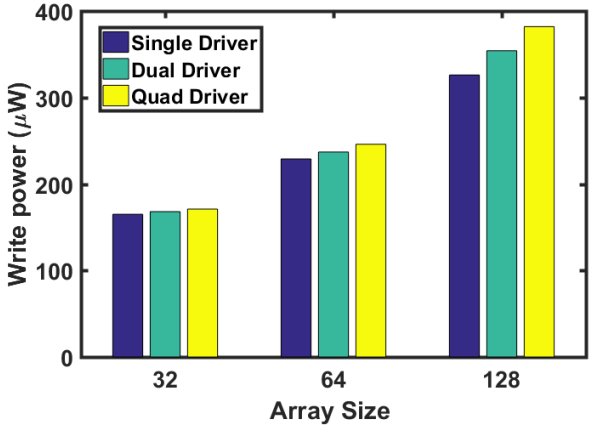

Figure 8: Write window vs. array size

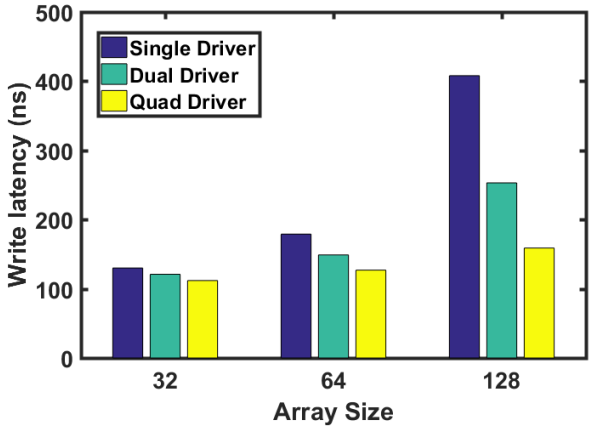

Figure 9: Write latency vs. array size

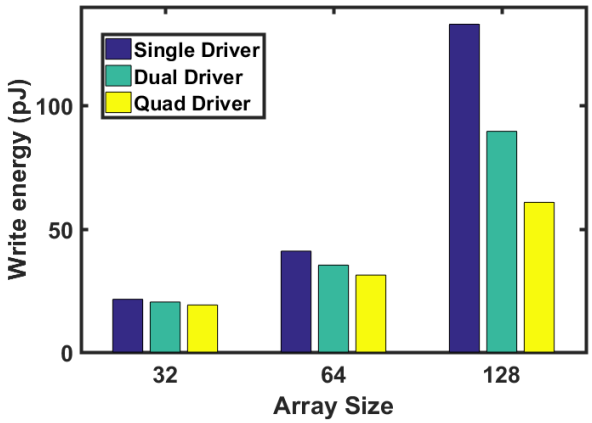

Figure 10: Write energy vs. array size

4. A 512X512 Crossbar array: A Case Study

A crossbar array is categorized as a subarray in a typical memory hierarchy [9]. Subarrays are often limited to 512X512 arrays. Hence, this section will investigate the impact of the proposed Multi-Driver write scheme on the reliability and efficiency of 512 X 512 crossbar arrays in order to provide a practical case study.

4.1. Reliability of the Crossbar array

Fig 9 depicts the voltage delivered across the selected cell $\boldsymbol{V_{cell}}$ and the maximum disturbance voltage across the unselected cell $\boldsymbol{V_{dis}}$ versus the write voltage. Here we depart from the write window FOM and choose to describe the write reliability in terms of write disturbance and voltage delivered across the selected cell separately. The threshold voltage of the series combination of the selector and the memory devices is also plotted and referred to as the cell threshold $\boldsymbol{V_t}$. To guarantee reliable write operation, the $\boldsymbol{V_{wr}}$ should be chosen such that $\boldsymbol{V_{dis}}$ is lower than the cell threshold voltage to avoid any write disturbance and, at the meantime, $\boldsymbol{V_{cell}}$ should exceed the cell threshold to effect a successful write operation on the selected cell. One can see the advantage of the Multi-Driver design over the conventional design approach. For example, using the Quad-Driver scheme, one can use a write voltage as low as 1.2V while maintaining low disturbance voltage. On the other hand, using the single driver approach requires write voltages as high as 2V. Although, all three schemes will effect a successful write operation at that voltage level, the disturbance voltage exceeds the cell threshold and, hence, a write disturbance occurs.

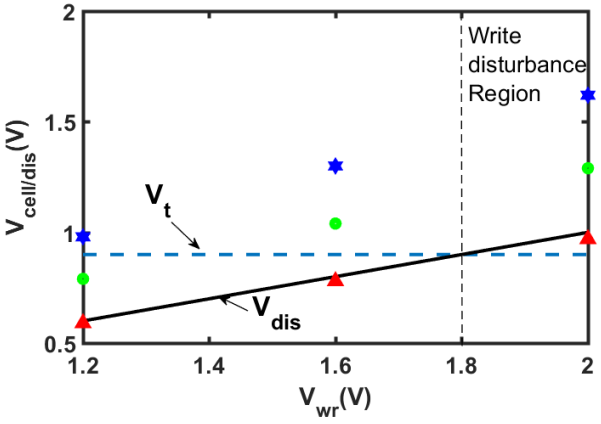

Figure 11: Voltage delivered across the worst case cell and write disturbance for 512X512 array.

4.2. Energy consumption of the crossbar array

Table 1 presents the results of four design examples with different write schemes for 512 X 512 arrays. The signal integrity is evaluated to ensure no write error has occurred. If a write error occurred, performance metrics are not reported. It is shown that employing more drivers help optimize the energy consumption of the crossbar array. Also, it should be noted that in some cases, increasing the write voltage might help improve the energy efficiency. For example, using the Quad-Driver scheme with write voltage 1.4V results in a lower energy consumption than using a write voltage of 1.2V due to the significant decrease in the write latency as explained earlier. Hence, the designer should optimize such parameters in order to achieve the best possible performance of the crossbar array.

Table 1: Case study for 512X512 array

Scheme	$\boldsymbol{V_{write}}$	$\boldsymbol{V_{dis}}$	W_{error}	P_{wr}	L_{wr}	E_{wr}
Single	2V	1V	Yes	-	-	-
Dual	1.6V	0.8 V	No	1.74mW	6.2us	10.7nJ
Quad*	1.4V	0.7 V	No	1.46mW	350ns	511pJ
Quad	1.2V	0.6 V	No	890uW	6.6us	5.9nJ

5. Conclusions

This work proposed a Multi-Driver write scheme that improves both signal integrity and energy efficiency of 1S1R ReRAM array. By employing multiple drivers, the effective line resistance of the crossbar array is reduced thereby enhancing the voltage delivered to the selected cell. This enhancement in voltage delivery improves both reliability and performance of the crossbar array via increasing the write window and reducing the energy consumption.

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