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Mesbah Uddin, and Garrett S. Rose

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A Practical Sense Amplifier Design for Memristive Crossbar Circuits (PUF)

Mesbah Uddin and Garrett S. Rose
Department of Electrical Engineering and Computer Science
University of Tennessee, Knoxville
Knoxville, Tennessee 37996-2250
Email: {muddin6, garose}@utk.edu

***Abstract*—As CMOS process scaling is nearing to an end, emerging non-volatile devices such as memristors have been explored extensively in circuit design due to their very low footprint, non-volatility and low power application. Memristors, however, display a wide variety of characteristics depending on their inter-lying materials, as is the case for any emerging nano-devices. In this paper, we have designed a sense amplifier which is well-suited to applications of HfO_x memristor based crossbar circuits. Specifically, we have successfully integrated this sense amplifier into our memristive crossbar physical unclonable function (PUF) as a part of our chip that we are fabricating. Our designed sense amplifier is able to operate reliably and reasonably fast at near-to-ground input and low supply voltage and with small voltage differences between the bit-lines. We have performed several Monte Carlo analysis to choose optimal design and device parameters and thus evaluated our proposed design for real hardware applications.**

I. Introduction

Memristors [1] have gained increased attention for the past few years because of their non-volatility, low switching energy, very low area and non-linear current-voltage characteristics. Here, we use the term 'memristor' to mean any of the metal-oxide semiconductors, transition metal-oxide, RRAM or ReRAM (resistive random access memory). Among the different memristor materials, HfO_x based memristors [2] are being explored by many groups due to their CMOS compatibility and very thin oxide layer implementation, among other advantages. Memristors can achieve a very high integration density within a crossbar architecture and thus memristive crossbars are being explored for memory and PUF circuits. In this work, we have designed and tuned our sense amplifier for a memristive crossbar PUF, the XbarPUF [3]. Specifically, we have designed a sense amplifier using 65nm CMOS process that is capable of operating with near-ground input voltages with small differences and with low supply voltage.

One of the major components in a dense memory architecture is the sense amplifier. The function of a sense amplifier is to sense voltage difference between two bit-lines of a memory and produce a full-swing rail-to-rail output during a memory read operation. For example, the sense amplifier can be used to determine a 1-bit response of the XbarPUF in place of an arbiter [4], [5]. A sense amplifier takes two column load voltages as its input bit-lines and determines which one is higher. Due to process variations in their respective memristive states and other parameters, memristors in two crossbar columns have slightly different memristance and thus have slightly different voltage drop at the series load resistance. The sense amplifier attached at the bottom of each pair of XbarPUF columns detects small differences in load voltages to produce a digital PUF response.

For this work, we have experimented with several sense amplifier designs. First, we have narrowed down topology choices based on our design requirements. Then we have analyzed the selected ones in terms of reliability, performance, and energy overhead. We have looked in the literature for a sense amplifier topology which best suits our design requirements and is compatible for integration with memristive circuits. Then we have modified that topology to work properly for our circuits. We have run several Monte Carlo analysis by varying transistor lengths, widths and supply voltage to find best circuit parameters in terms of speed, energy consumption and yield or reliability and determine the applicability of our proposed design in a real hardware.

The contributions of this work include: (1) identifying the design constraints of a sense amplifier for HfO_x memristor and its crossbar based PUF architecture and thus development of the proposed sense amplifier; (2) comparison of the proposed design with other conventional sense amplifier designs; (3) evaluation of the proposed design in real hardware by running Monte Carlo analysis; (4) improvement of the design parameters from Monte Carlo analysis; (5) trade-off analysis of different design choices using delay, power and chip yield.

The paper is organized as follows: section II surveys and shortly describes different sense amplifier design topologies that might be useful for memristive crossbar circuits. Section III explains the design requirements for this particular sense amplifier design for HfO_x memristor based crossbar PUFs. Section IV presents and discusses our proposed sense amplifier design in details. Section V presents the experimental results and provides the analyses and rationale for our work. Finally, future prospects and concluding remarks are provided in section VI and VII, respectively.

II. Background

Various types of sense amplifier (SA) topologies and designs have been considered for this work. We have built each type of SA circuit and analyzed them to evaluate their strengths and weaknesses with respect to our application. There are

mainly two common types of SA: current-mode and voltage-mode [6] and their many variations exist to suit the need of different applications. Simple modifications over these circuits are expected to match our design requirements.

Current latched sense amplifiers (CLSA) are widely used for their fast speed of operation [7]. In CLSA, two input voltages are applied to the gates of a pair of NMOS transistors. CLSA requires pre-charge which means their input bit-line voltages should be close to VDD to ensure that the transistors are in saturation when input are applied to their gates. The speed of operation of a CLSA, decreases fast with lower supply voltage and specially with lower bit-line voltages which drive the transistors out of saturation.

Voltage latched sense amplifiers or VLSA are another type of widely used sense amplifier design [6]. They are usually either on par or slower than CLSA in nominal supply voltages. However, VLSA is robust against V_t-mismatch (threshold voltage) and β-mismatch relative to other designs [8]. For both VLSA and CLSA, if the bit-line voltages are applied to gates of transistors, sensing would be slower if bit-line voltages are closer to GND rather than VDD (i.e. not precharged).

To deal with the high resolution requirement of memristor crossbar circuits, offset cancellation techniques are proposed in [9], [10]. However, they require capacitors which increase the sense amplifier area dramatically and also introduce further matching problems. SA designs suited for emerging devices e.g. MTJ (magnetic tunnel junction) have also been explored [11], [12]. Named as pre-charge sense amplifier (PCSA) [11], its circuit configuration is very simple and is quite fast. However, memristors, unlike MTJ can only be reliably read at low (subthreshold) voltage and thus integrating these SAs with any crossbar circuits like a XbarPUF or memory would be difficult. These circuits also do not provide rail-to-rail output unless higher supply voltage along with buffers are provided. They are also expected to be heavily affected by mismatch variation.

We have also considered and experimented with several other sense amplifier designs. However, a handful of those are operational based on our design requirements and, therefore, we have presented results and analyses for a chosen few designs.

III. Design requirements

HfO_2 memristors, such as those fabricated at SUNY-Poly, operate reliably at lower than 0.2V read voltage [2]. If the read voltage is higher than that, then the device retention characteristics is disturbed and a memristor can switch to either LRS (low resistance state) or HRS (high resistance state), given sufficient time. A crossbar PUF and memory have been designed with 0.4V READ voltage where the load resistor at the end of each crossbar column is chosen such a way that no more than 0.2V appears across a memristor. On-chip resistors may have high variance ($\sim$20% for nwell resistors of this 65nm technology) and having high voltage across them could result in a larger voltage variation in themselves than variation occurred by mismatch of memristors

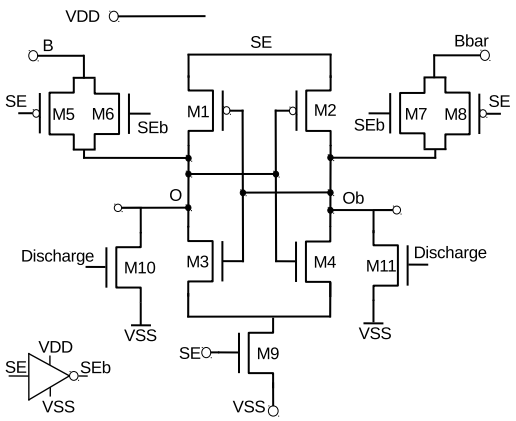

Fig. 1. Schematic diagram of the proposed sense amplifier design for memristor based crossbar architectures

with lower voltage across them. Therefore, to fight against such cases, lower READ voltage is a must, while maintaining maximum 0.2V across a memristor. This low READ voltage results in a pair of low bit-line input voltages for the sense amplifier. Having even lower supply voltage would reduce the sensing speed considerably and thus is not considered. The load-voltages or the effective bit-line voltages would be on the range of 100-250mV. More details on this memristor based PUF, the XbarPUF can be found in [5]. The clock frequency of the sensing is also determined by the memristor set-reset circuitries for the memristor PUF [5] and, therefore, can not be changed arbitrarily just for the sake of sense amplifier. In this work, clock period of 2μs or lower is considered. To reduce pin counts, only available on-chip supply voltages are considered. Since an SA would be needed for every pair of columns of a crossbar architecture, the area of the SA design should be as small as possible. Since these are hard requirements, we have to look for reasonably fast SA designs where the circuit works with supply voltage and low, out-of-saturation bit-line voltages with preferably high resolution.

To have a reliable sensing operation, any MOSFET mismatch should be negligible compared to the resolution of voltage difference between input bit-lines. V_t and β (sizing) mismatch, specifically among drive transistors of an SA reduce this resolution. These two mismatches are found to affect CLSA-based design more than VLSA [6]. As mentioned earlier, since the bit-line voltages are very low, applying them on transistors gates would make the sensing operation slower. On a different note, a memristor has very low equivalent capacitance, even lower compared to metal wires. Thus the whole memristor crossbar is assumed to be a resistive network with only wire capacitance. All these factors into our decision making for choosing our design to be based on VLSA.

IV. Proposed sense amplifier design

As mentioned previously, the driving factor behind choosing and designing an SA for memristive crossbars is a high-speed design capable of working with low (sub-threshold) VDD, bit-

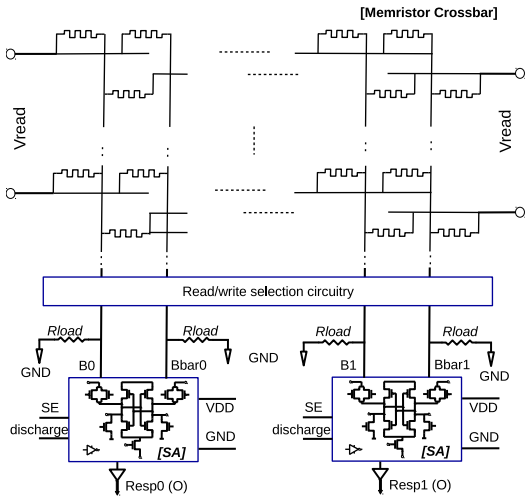

Fig. 2. Application of the proposed sense amplifier for a memristive crossbar PUF (XbarPUF [4])

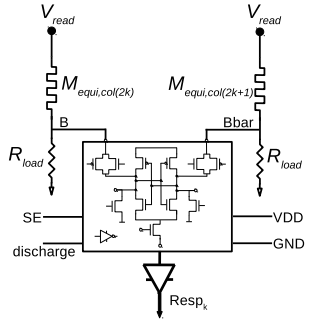

Fig. 3. An equivalent input-output circuit for our proposed sense amplifier in XbarPUF [4]

line voltages near to GND rail and with small voltage differences between those bit-lines. Available supply voltage and frequency choices are also limited. As we'll show later, VLSA works faster at low supply voltage and near-to-ground bit-lines than other sense-amplifier topologies, these requirements imply an SA design based on VLSA. The impact of threshold voltage (V_t) mismatch and beta-mismatch (β) are also low in VLSA than CLSA [6], [13] and that impact can be reduced further more reliably by increasing the transistor width in VLSA compared to CLSA. Lower mismatch means higher bit-line resolution and considering both the design requirements, we have chosen VLSA topology for our sense amplifier design. The schematic of our proposed sense amplifier design is shown in Fig. 1.

The input bit-line voltages are applied at diffusions of access transistors, M5-M8, in Fig. 1 and thus the SA circuit offers low input resistances to these bit-lines. The inputs are taken from the voltage division node between equivalent crossbar memristors and the series load resistance and, therefore, do not have infinite drive strength. If VDD is used, at the top of the design in Fig. 1 instead of 'SE' signal, VDD can affect through the PMOS transistors and affect/change the sampled voltage at nodes 'O' and 'Ob' during input sampling phase. Therefore, the most important modification compared to traditional VLSA has been done to detach the supply while sampling bit-line voltages into these internal nodes. The supply voltage of sensing PMOS transistors are tied to the sense enable signal, 'SE' in Fig. 1. Thus, when the SA is in sampling state, 'SE' remains low to ensure no current path is formed as well as voltage from the source of PMOS transistors do not interfere and change the latched voltage. During sensing, the signal 'SE' would provide power for the resolving of the two nodes 'O' and 'Ob'. Fig. 2 shows this application of our proposed SA design for the XbarPUF [5] when our SA is used to determine which crossbar column has higher voltage drop across its load resistor. Fig. 3 shows the input-output equivalent circuit for the SA during the response generation or 'read' operation of the XbarPUF. All memristors of a crossbar column form a resistor division circuit with the load resistor. The voltage from adjacent column load resistors are used as the two inputs to the sense amplifier as shown in Fig. 3. The sense amplifier compares and then produces a '1' or '0', full swing output. Additional buffers may also be used.

At low supply voltage, the time needed for latching of inputs to internal nodes of this type of SA become large and thus can dominate the overall performance. Unlike traditional VLSA, instead of using just NMOS or PMOS for access transistors, we have used both as transmission gates which increase the input voltage range of operation by passing analog input voltages reliably to internal nodes. Since our input voltages are near to GND, the NMOS transistors in the transmission gates are made stronger compared to PMOS ones.

Two additional NMOS transistors M10 and M11 are used to discharge the two internal sensing nodes 'O' and 'Ob', in Fig. 1. They discharge these nodes to zero or ground so that they do not add any bias to the next sensing operation. However, these two transistors are optional and can be omitted if at the end of sensing, two zero-input voltage are latched into these internal nodes, thereby reseting them. Moreover, for our XbarPUF application, response is generated only once during power-up and, therefore, there is no need for next sensing operation and thus we may totally omit this zeroing state. For other memristor crossbar architecture like an RRAM (memory), either these two transistors or a zeroing phase would be useful.

As a base, all transistor lengths are chosen to be at minimum length of L_{unit} = 60nm. Transistor widths are sized as follows: the four access transistors, M5-M8 in Fig. 1 are sized W_{unit} = 1.2μm each, top two PMOS transistors, M1-M2 are also sized 1.2μm while M3-M4 are sized 2*W_{unit} = 2.4μm. With equal sizes, NMOS access transistors are actually stronger than PMOS access transistors which is desirable since the two bit-line voltages to be sampled are closer to ground than to VDD. Their sizes are also chosen to be large enough to have negligible drop across them. M1-M4 transistors forms two equal sized cross-coupled inverters where NMOS are made stronger. The two discharge transistors, M10 and M11 are sized with 2.4μm to have a fast recharge phase as well as quick discharge of both nodes (close to ground). The lone inverter, in Fig. 1 and if any additional buffers used are sized properly to comply with the input and output load demands

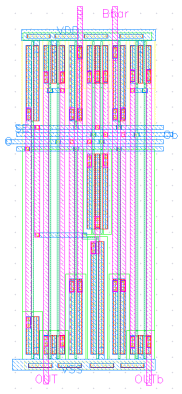

Fig. 4. Layout of the proposed sense amplifier done using 65nm technology (Dim: 10.9μm×4.2μm)

and are usually a few times larger than minimum. All these sizes might be scaled up to reduce mismatch and improve yield as we have shown later.

There are three states of operation for this sense amplifier based crossbar PUF or memory design. During the READ phase, sense enable signal, 'SE' of Fig. 1 is kept low. This is the input voltage sampling state where voltage across column load resistors are sampled into sense amp's internal nodes 'O' and 'Ob'. During the next sensing phase, signal 'SE' is enabled high and thus supply is enabled and bottom NMOS transistor is turned on as well to ensure a path from VDD (high SE) to GND. The node with higher voltage resolves to VDD while the other node resolves to GND. The signal, 'SE' should be kept high during this whole time which provides the power for the sensing operation. In last or third phase, both internal nodes 'O' and 'Ob' are discharged to ground to make the sense amplifier ready for next sensing operation. A small spike of around 50ns pulse is applied at the gates of discharge transistors for this purpose. Equal-sized buffers or buffer-chains can be used to separate the internal output nodes, 'O' and 'Ob' from outside and to be able to drive larger load. Buffers add zero or negligible delay due to relatively slower rising or falling nature of internal output nodes during sensing phase compared to the rise/fall time of inverters in buffers.

Fig. 4 shows the layout for this proposed SA plus two output buffers. Since this is for the XbarPUF, discharge transistors are not used in this particular layout. The layout of the SA is made symmetric for the cross-coupled inverters to remove any bias to any input bit-lines. Internal connections and wire lengths and widths are designed such a way that both 'O' and 'Ob' nodes have the same output load. One important thing is that the SA layout is intentionally made taller rather than a wide multi-finger design for the sake of crossbar circuits. Because an SA is needed for each pair of columns of an XbarPUF as shown in Fig. 2, wide SAs would eventually increase the overall pitch of the memristor crossbar and thus each SA should be as narrow as possible without degrading performance. This design is being fabricated now and there is also a guard ring around each SA on the chip to mitigate noise from other circuit components. As analyzed in [13], finger

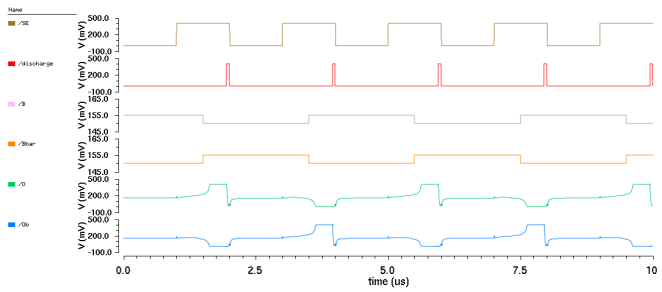

Fig. 5. Waveforms for transient simulation of proposed SA for input bit-line voltages of 150mV and 155mV with VDD = 0.4V

numbers or sizes do not affect VLSA-based designs and thus our choice of finger widths is only to keep low aspect ratio and minimize area and comply with the pitch of the attached memristor crossbar.

TABLE I
COMPARISONS AMONG DIFFERENT SA TOPOLOGIES

Topology	Conventional (CLSA) [7]	VLSA [14]	PCSA [11]	Proposed
Precharge needed	yes/no	yes	no	no
Avg. delay (μs)	2.75	3.51	0.62	0.27
Avg. power (nW)	0.48	0.77	0.42	0.63 / 0.19

V. RESULTS, ANALYSES AND DISCUSSION

As mentioned in last section, fast operation under low supply voltage with low input bit-line voltages, high resolution of bit-line voltage difference, and compatibility with memristor crossbar architectures are the driving forces behind choosing our particular SA design. We have built and experimented with different SA circuit topologies and compared against our design. Table I lists the comparison among different SA designs where the supply or VDD is kept at 0.4V and bit-line voltages are 150mV and 155mV. For fair comparison, for each of the design, same unit length (60nm) and width (1.2μm) are used to generate the data for this table. It can be seen that our proposed design is by far the fastest among them. Both the CLSA [7] and VLSA [14] work very slowly at this bit-line voltage range. The PCSA (pre-charge SA) from [11] consumes smaller power with relatively high speed. Our proposed design has comparatively high power consumption when discharge transistors are used. However, without those two, our proposed design has also the lowest power consumption among these designs. The power consumption of Table I includes dynamic power of inverter and power consumption during all phases of the SA. Another thing to note is that because of the high delay of some of these designs, the results of Table I are generated using a lower frequency with clock period of 12μs instead of the required maximum of 2μs. Therefore, actual power consumption would be higher.

Fig. 5 displays the waveforms for our implemented SA design at 0.4V VDD with bit-line voltages of 150mV and 155mV ('B' and 'Bbar' in Fig. 1). The clock or sense enable signal 'SE' has a period of 2μs. The value of the input signals

TABLE II
PERCENT YIELD OF PROPOSED SENSE AMPLIFIER FOR DIFFERENT TRANSISTOR SIZES AND SUPPLY VOLTAGE

Transistor sizes	$(\frac{W}{L})$	$(\frac{W}{3L})$	$(\frac{3W}{3L})$	$(\frac{2W}{5L})$	$(\frac{5W}{5L})$
VDD = 0.4V	67.35	72.45	78.55	83.25	87.20
VDD = 0.6V	64.20	77.20	89.70	90.70	98.50
VDD = 0.9V	61.10	73.10	84.70	87.00	95.50
VDD = 1.2V	60.50	72.70	84.30	87.20	95.40

'B' and 'Bbar' are flipped on each clock cycle to see if our design can resolve to opposite values quickly. A discharge signal of $50n$s duty cycle with same 2μs time period is used to discharge the output nodes 'O' and 'Ob' at the end of each sensing phase. During sensing ('SE' goes high), 'O' and 'Ob' resolves either VDD or GND, based on which of the 'B' or 'Bbar' signal is high. The output is valid before discharge signal is high and a sufficient delay after 'SE' goes high. Outputs should be alternating on each cycle with 'O' and 'Ob' of resolving to opposite values and that is what it can be seen in Fig. 5.

We have run Monte Carlo analysis to determine the reliability of the proposed design. For each Monte Carlo run, we have applied two input pairs, one where output should be a '1' and one where output is a '0'. The clock period is chosen to be 2μs with 50% duty cycle, suitable for the XbarPUF. Thus 1μs is being alloted for sensing phase plus a $50n$s discharge phase. The input voltages are 150mV and 155mV initially, flipped on the second cycle to get both a '1' and '0' output on consecutive cycles. The supply voltage and widths and lengths of the transistors are varied for different runs. To determine the best circuit parameters i.e. length and width of each transistor and the supply voltage, we have run Monte Carlo analysis for 500 chips for our proposed design with different (W/L) ratios and different supply voltages. Here in the table, W = W_{unit} = 1.2μm and L = L_{unit} = 60nm (min. length of this 65nm technology). As expected, increasing the length and (W/L) ratio increase transistor area and thus reduce mismatch, thereby improves the yield of the design considerably. It can also be seen from Table II that with increasing VDD, yield decreases. It can be explained by the fact that input voltages are close to GND and, therefore, with higher VDD, there is a higher magnitude of leakage which corrupts output nodes at the start of sensing and just after latching of input to those nodes, thereby reducing yield. However, with a sub-threshold VDD (at 0.4V VDD where for this technology, V_{th} is around 500-550mV), the delay is longer while clock frequency is unchanged and, therefore, it may not resolve for all cases due to additional delay arising from mismatch. Thus, at 0.4V, our design has the lowest yield compared to above-threshold supply voltages as in many instances the SA doesn't get enough time to give a full-swing output. Although for the leftmost column of transistors with unit length (60nm), yield is actually highest for 0.4V VDD. The reason is that SA operates very fast with transistor length being very small and thus decreasing effect of additional mismatch delay is less than the yield improvement achieved by lowering VDD. From Table II, it can be concluded that for overall better yield ($\geq$80-85%), larger transistor sizes (rightmost three columns of Table II) should be considered.

TABLE III
SENSING DELAY (nS) OF PROPOSED SENSE AMPLIFIER FOR DIFFERENT TRANSISTOR SIZES AND SUPPLY VOLTAGE

Transistor sizes	$(\frac{3W}{3L})$	$(\frac{2W}{5L})$	$(\frac{5W}{5L})$
VDD = 0.4V	712	625	627
VDD = 0.6V	19.63	16.7	16.7
VDD = 0.9V	1.02	1.524	1.523

TABLE IV
ENERGY(JOULE) PER CYCLE OF PROPOSED SENSE AMPLIFIER FOR DIFFERENT TRANSISTOR SIZES AND SUPPLY VOLTAGE

Transistor sizes	$(\frac{3W}{3L})$	$(\frac{2W}{5L})$	$(\frac{5W}{5L})$
VDD = 0.4V	20.66f	16.79f	41.79f
VDD = 0.6V	0.80p	0.50p	1.26p
VDD = 0.9V	11.08p	5.54p	13.65p

Larger transistor sizes reduce mismatch and thus improve yield, but they also contribute to larger area, delay and energy overhead. Therefore, there is a trade-off between yield and delay plus energy overhead of the circuit. To find delay and energy consumption, we have experimented with the transistor sizes listed in Table II, except for the (W/L) and (W/3L) as their yield are too low and thus are not considered for further analysis. A VDD of 1.2V is not also considered as it increases the power consumption considerably. Table III lists the sensing delay for the selected three transistor sizes with relative better yield where Table IV lists the total energy consumption during one cycle of the designed SA. From these two tables, it can be found that transistor size of (2W/5L) i.e. 240μm width and 300nm length gives a much lower sensing delay as well as low conversion energy at 0.6V VDD, compared to other. Its area and leakage should also be lower compared to the other two sizes as width and (W/L) ratio are smaller. However, depending on the design requirements and application, a trade-off among yield, delay, energy consumption and total area can be easily made from these analysis.

VI. FUTURE WORK

We have implemented our sense amplifier in a chip designed with 65nm process. After fabrication, we can get the actual characteristics from this circuit implementation. An XbarPUF which uses a few of these sense amplifiers is also being fabricated. Therefore, the next step after getting that chip back is to measure SA performance in a real application on a fabricated chip. We can also measure and analyze performance change due to mismatch from manufacturing variations or variations due to temperature, aging, supply rail noise or any other environmental factors from the implementation.

VII. CONCLUSION

The whole schematic and layout design has been done using Cadence Virtuoso with 65nm technology. Even though

65nm process can be considered small for analog design, we choose 65nm process for this design as well to comply with other circuit components of our whole work there. As this sense amplifier is designed primarily for memristor based crossbar circuits, new design constraints are imposed compared to any traditional CMOS analog circuits. The layout is drawn manually and is symmetric to both the inputs and outputs and therefore, our proposed design actually is shown to resolve very small input voltage differences pretty fast. The validity and effectiveness of our proposed design in a practical application is validated by several different Monte Carlo runs. These Monte Carlo runs help to gather insights about the circuit parameters to choose them more wisely.

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