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2018 IEEE Dallas Circuits and Systems (DCAS) Conference, Dallas, TX, Nov 2018.

The online home for this paper may be found at: http://web.eecs.utk.edu/ grose4/

Citation Information (BibTex):

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@INPROCEEDINGS{hasan2018mos,
  author=" Md Sakib Hasan and Ifana Mahbub and Syed K. Islam
and Garrett S. Rose",
  title="A MOS-JFET Macromodel of SOI Four-Gate Transistors
(G4FET) to Aid Innovative Circuit Design",
  booktitle="{IEEE} 13th Dallas Circuits and Systems
Conference {DCAS}",
  month="November",
  year="2018",
  pages="1-4",
  address="Dallas, TX, USA"
}
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A MOS-JFET Macromodel of SOI Four-Gate Transistors (G^4FET) to Aid Innovative Circuit Design

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***Abstract*—A MOS-JFET macromodel of silicon-on-insulator (SOI) four-gate transistor (G^4FET) is presented in this paper to facilitate innovative circuit design with this novel multi-gate transistor. Designing interesting and innovative circuits with any new device requires a SPICE model that will work sufficiently well throughout the desired operating regions. A macromodel approach is adopted in this work which can provide a reasonably fast and accurate circuit simulation. Since G^4FET combines the functionality of MOSFET and JFET devcies and robust, fast and reliable models of both MOSFET and JFET are already available, a macromodel combining these existing models is desirable from the perspective of a circuit designer. The model captures the essential interaction between multiple gates and accounts for both the volume and the surface conduction. In order to justify the feasibility of the macromodel, it is used to simulate two analog multiplier circuits which have been previously demonstrated experimentally and the simulation results match quite well with experimental findings.**

I. Introduction

The amazing technological advancements in semiconductor industries, dictated by the desire to follow Moore's Law, have resulted in the rapid scaling down of silicon transistors over the past several decades. However, bulk silicon devices are now faced with some fundamental physical limits. Some of the non-idealities such as subthreshold conduction, gate oxide leakage and reverse-biased junction leakage can no longer be ignored. Researchers have been looking for new process technologies which can solve the problems associated with bulk silicon scaling and enable the semiconductor industry to extend Moore's Law in the foreseeable future. A promising candidate is silicon-on-insulator (SOI) technology which offers many advantages such as ideal device isolation, reduced parasitic capacitance, excellent sub-threshold slope, elimination of latch up, increased switching speed, radiation hardness, reduced leakage current etc. [1]. One of the recent SOI devices with multiple gates that has been shown to be a potential candidate for innovative circuit design is G^4FET [2]. The name G^4FET is derived from its four independent gates, two providing vertical MOS (metal-oxide-semiconductor) field-effect action while the other two gates providing lateral junction field effect transistor (JFET) functionality in a single silicon body. G^4FET with its unique structure is a promising candidate for different analog, mixed-signal and digital applications with significantly reduced transistor counts. Some applications have already been experimentally demonstrated including LC oscillators and Schmitt trigger circuits using negative differential resistance [3], four quadrant analog multipliers [4], adjustable threshold inverters, universal and programmable logic gate capable of highly efficient full adder design [5] etc. Another possible application is the formation of quantum wire with low subthreshold swing, high mobility and low noise in depletion-all-around action when the vertical MOS gates and lateral JFET gates are used simultaneously to create a conducting channel surrounded by depletion regions. G^4FET inspired multiple state electrostatically formed nanowires have already been used for threshold logic functions [6] and high-sensitivity gas sensing [7].

A G^4FET transistor can be used in several different operating regimes depending on the bias voltages on its four gates and the silicon epi layer thickness. A number of works ([8], [9], [10], [11]) based on experimental results, analytical explanation and numerical simulation have been reported in the literature to explore these operating conditions. To use G^4FETs for circuit design, a reasonably fast and accurate SPICE model is required that will work sufficiently well throughout the different operating regions corresponding to different gate biases and can be used for DC, transient and AC simulation. So far, it has not been possible to come up with such a compact model based on device physics. Although it is theoretically possible to solve coupled non-linear differential equations to explore different operating conditions, this will take an excessive amount of time making it unsuitable for useful circuit design. However, G^4FET has also been called MOSJFET [2] since it combines both metal-oxide-semiconductor field-effect transistor (MOSFET) and junction field-effect transistor (JFET) actions in a single silicon island. This is the motivation behind the macromodel approach presented in this work where existing MOSFET and JFET models are combined to build the macromodel where the interactions between different gates are modeled using analytical expression derived from device physics.

The remainder of the paper is as follows: Section II describes

978-1-5386-9262-2/18/$31.00

the device structure and operating principle of G^{4}FET. Section III goes through the model development and SPICE implementation. Section IV shows the results from circuit simulation for two analog multiplier circuits using G^{4}FET and validates the model by comparison with experimental results. Finally, section V concludes the paper with a summary of the work.

II. Device structure and operation

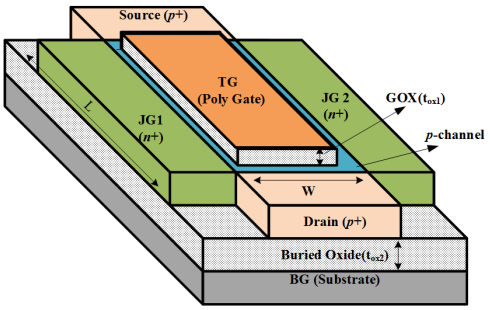


Fig. 1: 3-D structure of a *p*-channel G^{4}FET

G^{4}FETs can be fabricated in either partially or fully-depleted SOI (PD/FD-SOI) process. It has four independent gates for modulating channel conduction. There are two lateral junction-gates which act like JFET gates and two vertical oxide gates which act like MOS gates. G^{4}FET is a majority carrier device in which a regular *n*-channel SOI MOSFET with two body contacts on the opposite sides of the channel works as an *p*-channel G^{4}FET. The *n*+ doped source and drain of the MOSFET function as lateral junction-gates. They are used like JFET gates to control the channel conduction width. The top oxide gate works like a classical MOS gate whereas the buried oxide along with the substrate biasing acts as a bottom-gate. These vertical gates are used to create the accumulation/ depletion/ inversion of free carriers in the silicon epi layer near the top and the bottom oxide interfaces. The body contacts are highly doped to make ohmic contact with the channel and are used as the source and the drain for the *p*-channel G^{4}FET. An accumulation/depletion-mode *p*-channel G^{4}FET is thus realized from an inversion-mode, *n*- channel MOSFET. Similarly, a *n*-channel G^{4}FET can be constructed from a conventional SOI *p*-channel MOSFET. Fig. 1 shows the 3-D structure of an *p*-channel G^{4}FET. It is evident that no specialized fabrication procedure is necessary for this device.

III. Model development

G^{4}FET combines MOS and JFET actions by supporting both surface and volume conduction. The top and the bottom oxide gates provide MOS action whereas the lateral junction-gates work like JFET. The threshold voltage of the top and the bottom-gates are influenced by the junction-gate voltage. It can be considered as a combination of two MOSFETs (surface conduction) working in parallel with a JFET (volume conduction).The direction of current flow is perpendicular to the conventional MOSFET. The length and the width of the G^{4}FET are the width and the length of the original MOSFET, respectively. There can be three conduction paths, namely, 1) top surface conduction near gate oxide interface, 2) bottom surface conduction near buried oxide interface and 3) volume conduction away from vertical oxide interfaces. Some of the terms used in the model are introduced below:

Junction-gate capacitance $C_{JG} = \frac{\epsilon_{Si}}{W}$, top oxide capacitance $C_{ox1} = \frac{\epsilon_{ox}}{t_{ox1}}$, bottom oxide capacitance $C_{ox2} = \frac{\epsilon_{ox}}{t_{ox2}}$, $\phi_F = -V_T ln(N_d/n_i), \phi_b = E_g/2 + V_T ln(N_d/n_i), V_P = \phi_b - (qN_dW^2)/(8\epsilon_{Si})$, top-gate threshold voltage$= V_{TH}$, the bottom-gate voltage causing the onset of accumulation and inversion at the bottom-gate are V_{BG}^{acc} and V_{BG}^{inv}, respectively. Three geometry dependent parameters are,

$$\alpha = (2\sqrt{2})/tanh(2\sqrt{2}t_{Si}/W)$$

$$\beta = \frac{\frac{\gamma C_{JG}}{C_{ox1}}}{1+\frac{\alpha C_{JG}}{C_{ox2}}}$$

$$\gamma = (2\sqrt{2})/sinh(2\sqrt{2}t_{Si}/W)$$

Here, W is the width of the transistor, t_{Si} is the silicon film thickness, t_{ox1} is the top oxide thickness, t_{ox2} is the buried oxide thickness, $V_T = kT/q$ is the thermal voltage, N_d is the donor concentration in the body, n_i is the intrinsic carrier concentration, E_g is silicon bandgap, ϵ_{Si} is the permittivity of silicon, and ϵ_{ox} is the permittivity of silicon dioxide.

The onset voltage of accumulation and inversion for the bottom-gate, V_{BG}^{acc} and V_{BG}^{inv}, can be expressed [10] as,

$$V_{BG}^{acc} = V_{FB2} + (\gamma - \alpha)(V_{JG} - V_P)\frac{C_{JG}}{C_{ox2}} \tag{1}$$

$$V_{BG}^{inv} = V_{FB2} + (1 + \alpha C_{JG}/C_{ox2})2\phi_F - V_P(\gamma - \alpha)C_{JG}/C_{ox2} + (1 + \gamma C_{JG}/C_{ox2})V_{JG} \tag{2}$$

The bottom gate may be accumulated, depleted or inverted. When the bottom-gate is in inversion i.e. $V_{BG} < V_{BG}^{inv}$,

$$V_{TH} = V_{FB1} - \gamma(C_{JG}/C_{ox1})(2\phi_F + V_P) - \alpha(C_{JG}/C_{ox1})(V_{JG} - V_P) \tag{3}$$

When the bottom-gate is depleted i.e. $V_{BG}^{inv} < V_{BG} < V_{BG}^{acc}$,

$$V_{TH} = V_{FB1} - \beta(V_{BG} - V_{FB2}) + (\gamma - \alpha)(C_{JG}/C_{ox1} + \beta C_{JG}/C_{ox2})(V_{JG} - V_P) \tag{4}$$

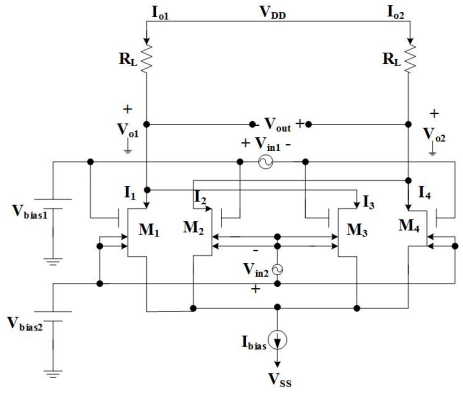
When the bottom-gate is in accumulation i.e. $V_{BG} > V_{BG}^{acc}$,

$$V_{TH} = V_{FB1} + (\gamma - \alpha)(C_{JG}/C_{ox1})(V_{JG} - V_P) \tag{5}$$

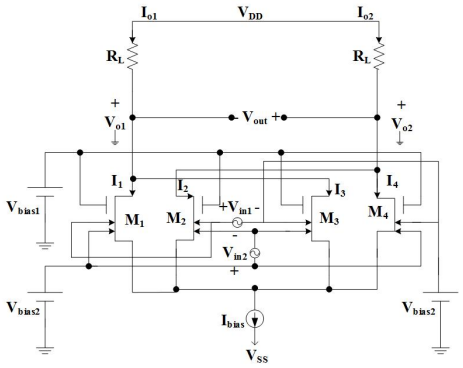
Here, V_{FB1} and V_{FB2} are the flat band voltages of the top-gate and the bottom gates, respectively. Based on the above relationships among different gates, a macromodel is created combining conventional SPICE Level-1 MOSFET and JFET models. Of course, the model can be further improved by using higher level MOSFET models such as Level-2/3

and BSIM/BSIMSOI models for deep submicron devices. The simple model is used here to show the feasibility of the macromodel by demonstrating its effectiveness in capturing the essence of the complex interaction between multiple gates. Since the accumulated back gate provides a shunt leakage conduction path which is undesirable for most applications, it is assumed that the back gate is never accumulated and the condition for depleted or inverted back surface is considered. The top surface conduction is modeled using a MOSFET and the volume conduction is modeled using a JFET. However, instead of a constant threshold MOSFET, the model allows for threshold voltage modification based on multiple gate biases using the relationship described in Eq. 1- 5.

IV. Model Validation



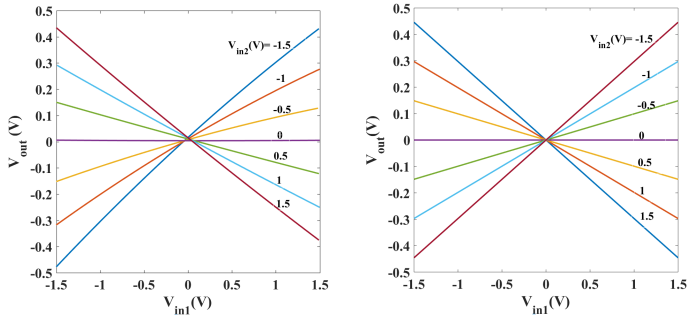
(a)



(b)

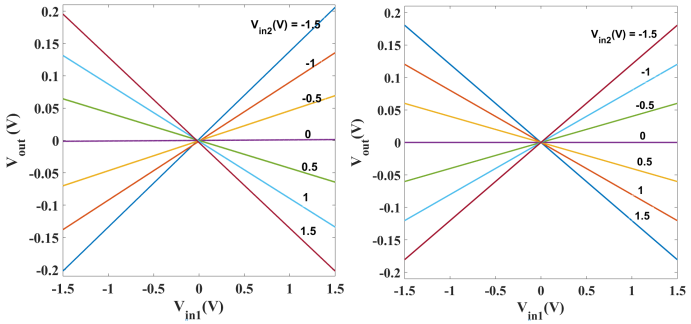
Fig. 2: Analog Multiplier with four G^{4}FETs, (a) Configuration 1, b) Configuration 2 [11].

The developed macromodel has been implemented in SPICE simulator as a subcircuit and validated against experimental results obtained from two four-quadrant analog multiplier circuits. The independent multi-gate current modulation capability of G^{4}FET can be used to design analog multiplier with only four transistors and two different configurations were experimentally demonstrated in [4]. Both of them have multiplier core made of four G^{4}FETs biased by a constant current sink and loaded by same resistors R_L which convert the differential output current to a differential output voltage. However, the input is different for these two cases. As shown in Fig. 2a, configuration 1 has one input V_{in1} at the top-gate and other input V_{in2} at the junction-gates, which are tied together. In configuration 2, shown in Fig. 2b, two differential input voltages V_{in1} and V_{in2} are connected to two lateral junction-gates, whereas the top-gate is biased at a constant voltage.



(a) (b)

Fig. 3: DC transfer characteristic for Configuration 1, a) Experimental, b) Simulation.



(a) (b)

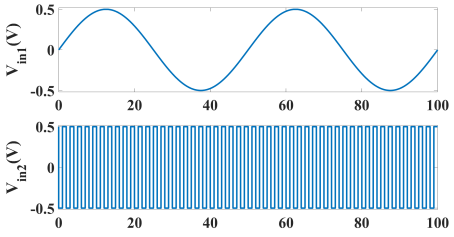
Fig. 4: DC transfer characteristic for Configuration 2, a) Experimental, b) Simulation.

The macromodel was used to simulate both the configurations. DC transfer characteristic for configuration 1 and configuration 2 are shown in Fig. 3 and 4, respectively. The measurement results are shown in Fig. 3a and Fig. 4a whereas simulation results obtained using the macromodel are shown in Fig. 3b and Fig. 4b, respectively. Table I give a quantitative comparison between DC transfer characteristics from measurement and simulation results for both configurations. The figures and the table show that the model captures the DC transfer characteristics quite well.

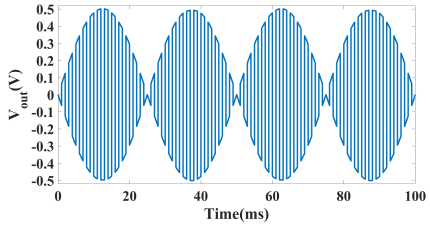
Fig. 5 shows the result for configuration 1 as an analog multiplier where the inputs are a 20 Hz, 1 Vp-p sinusoidal-wave and a 500 Hz, 1 Vp-p square-wave. The simulation result using the macromodel in Figure 5.6 (b) shows good matching with the experimental result [4]. The peak-to-peak output voltage in simulation is 1.0025 V which is very close to the measurement result of 1 V, with a relative error of 0.25 %.

TABLE I: Comparison between experimental and simulation results for DC transfer characteristics

V_{in2} (V)	Configuration 1, $V_{out(p-p)}$ (V)			Configuration 2, $V_{out(p-p)}$ (V)		
	Experimental	Simulation	Error(%)	Experimental	Simulation	Error(%)
−1.5	0.91	0.89	2.09	0.41	0.36	11.52
−1	0.59	0.59	0	0.274	0.241	12.04
−0.5	0.281	0.297	5.69	0.139	0.12	13.67
0	0	0	0	0	0	0
0.5	0.273	0.297	8.79	0.129	0.12	6.98
1	0.54	0.59	9.19	0.27	0.24	9.06
1.5	0.81	0.89	9.72	0.4	0.36	9.3



(a)



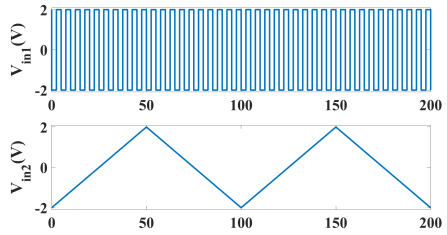
(b)

Fig. 5: Transient simulation results with analog multiplier for configuration 1, a) inputs, b) output.

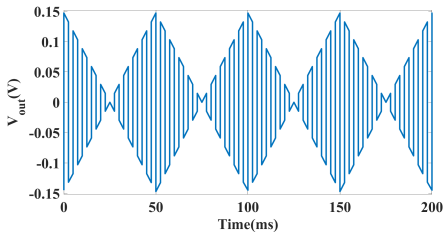
Configuration 2 was also used as an analog multiplier with two different input signals; a 10 Hz, 4 Vp-p triangular-wave and a 200 Hz, 4 Vp-p square-wave. This configuration has a reduced gain compared to configuration 1, but it has a higher input voltage swing capability. Fig. 6 shows the simulation results. There is a reasonable agreement in peak-to-peak output voltage between simulation results of 0.294 V and experimental measurements of 0.3 V [4], with a relative error of 2%.

V. Conclusion

The macromodel of G^{4}FET captures some of the underlying physics of G^{4}FET operation and effectively combines MOSFET and JFET functionalities into a single model. The availability of robust, fast and accurate MOSFET and JFET SPICE models facilitates faster implementation in circuit simulator. The model has been successful in reproducing experimental results from two analog multiplier circuits. Since this model captures the essential interplay between multiple gates, it has the potential to enable circuit designers to come up with new interesting analog and digital circuits using G^{4}FETs. In this work, the macromodel has been developed with Level 1 SPICE models to show the feasibility of such an approach. Further improvements in accuracy can be accomplished using higher level models with a few optimized fitting parameters.



(a)



(b)

Fig. 6: Transient simulation results with analog multiplier for configuration 2, a) inputs, b) output.

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